become difficult, accompanying an improvement in speed of a microcomputer or a multi-bit bus. Furthermore, the various functions for system realization, other than a microcomputer, are embedded in LSI in a system LSI in which a microcomputer is embedded, so that it has become difficult to emulate the original function which the terminal used as an address bus or a data bus for connection with the memory of ICE has, using the ICE.

Replace the paragraph beginning at page 2, line 15 with:

The debugging circuit performing the function, which the ICE conventionally has on the basis of the foregoing description, is embedded in a microcomputer, and a program development technique has been adopted such that the emulator (debugger) is connected to a host computer through an LSI terminal only used for debugging.

Replace the paragraph beginning at page 2, line 21 with:

Fig. 6 shows an internal circuit arrangement of the conventional microcomputer-embedded LSI 1. Reference numeral 2 denotes a bus interface. Reference numeral 3 denotes a CPU. Reference numeral 4 denotes a memory. Reference numeral 5 denotes a debugging circuit. Reference numeral 6 denotes a trace circuit in the debugging circuit. Reference numeral 7 denotes a control circuit (event control circuit). Reference numeral 8 denotes a trace buffer memory. Reference numeral 9 denotes an output latching circuit. Reference numeral 10 denotes an output control circuit. Reference numeral 11 denotes a control bus. Reference numeral 12 denotes an address bus. Reference numeral 13 denotes a data bus. Reference numeral 14 denotes a control bus. Reference numeral 15 denotes an address bus. Reference numeral 16 denotes a data bus. Reference numerals 14, 15 and 16 denote trace buses. Data is output from the trace circuit 6 through the LSI data output terminal DATA. This data is constituted by 4 bits.

Replace the paragraph beginning at page 3, line 14 with:

Fig. 7 shows a timing chart of various signals in this trace circuit 6. Any desired data (8 bits) of the control bus 14, the address bus 15, and the data bus 16 is stored in the trace buffer memory 8 through the event control circuit 7 based on a signal WRITE that is synchronized with the bus clock signal CK. The data once D stored in the trace buffer memory 8 is output, based on subsequent READ signals, from the trace buffer memory 8 to the output latch circuit 9 and is further input into the output control circuit 10. The output control circuit 10 converts 8-bit data to 4-bit data, which is output through the terminal DATA, using the output control signals S1 and S2, each of whose frequency is the same as

the bus clock signal CK frequency and whose phase is shifted by only π through the terminal DATA. In Fig. 7, ABh, CDh, 12h, 34h are hexadecimal numbers. Furthermore, in Fig. 6 and Fig. 7, A1, A2, A3, and A4 are 8-bit data stored in sequence in the trace buffer memory 8.

Replace the paragraph beginning at page 4, line 6 with:

However, the processing speed of the microcomputer in the system LSI in recent years is becoming faster and the bus clock frequency therein is increasing. As a result, in the conventional case, access speed to a trace buffer memory cannot catch up with the speed at which data is transmitted from the control circuit. In other words, since one bus cycle is becoming shorter and shorter, it is becoming difficult to store the input data in the trace buffer memory or to output the data from it during one bus cycle.

Replace the paragraph beginning at page 5, line 15 with:

Fig. 2 shows time charts of various signals for explaining operation of the first embodiment.

Replace the paragraph beginning at page 5, line 17 with:

Fig. 3 shows time charts of various signals for explaining operation of the second embodiment of this invention.

Replace the paragraph beginning at page 5, line 22 with:

Fig. 5 shows time charts of various signals for explaining operation of the third embodiment.

Replace the paragraph beginning at page 6, line 1 with:

Fig. 7 shows time charts of various signals for explaining operation of the conventional circuit.